

Application No.: 09/864,561

5

Docket No.: 08211/000S081-US0

REMARKS


Claims 1-7 and 9-20 are pending in this Application. The Office Action mailed December 5, 2003, has rejected Claims 1-7 and 9-20. No Claims were objected to. In response, Applicant has amended Claims 1, 7, and 13 to further clarify the patentable subject matter of the claimed invention. No Claims have been cancelled. No new matter has been added by any of these amendments. For the reasons discussed in detail below, Applicant submits that the pending claims are patentable over the art of record.

The 35 U.S.C. §103(a) rejection of Claims 1-4, 7, and 11-16:

Paragraph 3 of the Office Action has rejected Claims 1-4, 7, and 11-16 under 35 U.S.C. §103(a) as being unpatentable over US Patent Application 2002/0036723 by Ishii et al (hereinafter "Ishii") in view of U.S. Patent No. 5,287,100 to Guttag et al. (hereinafter "Guttag"). Applicant respectfully traverses this rejection.

The Applicant respectfully submits that the prior art references do not suggest or teach any of the claimed limitations. The present invention is directed to solving the problem of beat patterns in video signals. This problem is related to video pixel frequency and interference from other system frequencies. In a video display sub-system, these interferences alter slightly the width of the pulse created by the video pixel clock, which produces beat patterns. See Specification, Page 3, line 26 - Page 4, line 4. The present invention aims to solve this problem by using a "clean" local pixel clock to re-clock the video data at a final stage of a video path to the DAC's. See Specification, Page 5, lines 8-10.

Amended Claim 1 recites a method for clocking video data to reduce beat patterns, comprising *inter alia* providing a local clock signal to re-clock the video data signal at a final stage of a video path between the video data signal circuitry and output circuitry, the local clock signal being based on the external clock reference, thereby removing interfering influence of other clock signals on the predetermined pixel frequency.

{S:\8211\000s081-us0\80003753.DOC  }

Application No.: 09/864,561

6

Docket No.: 08211/000S081-US0

Unlike the claimed invention, Ishii discloses an apparatus for correction of convergence and distortion by correcting the position errors of the three colors red, blue, and green. See Ishii, Abstract, Par. 44, Fig. 5A. In particular, Ishii proposes a clock generation circuit for generating three different clock circuits in front of a video circuit. See Ishii, Par. 46, 52, Fig. 6. As the Office Action correctly states, Ishii does not teach or suggest a clock signal to re-clock the video data signal between the video data signal circuitry and output circuitry based on an external clock. Furthermore, Ishii does not teach or suggest providing the clock signal at a final stage of a video path. Therefore, Ishii does not teach or suggest the claimed invention as recited in amended Claim 1.

Gutttag discloses an integrated circuit for use with a plurality of clock oscillators. See Gutttag, Abstract. However, Gutttag does not teach or suggest providing a local clock signal to re-clock the video data signal at a final stage of a video path between the video data signal circuitry and output circuitry, the local clock signal being based on the external clock reference, thereby removing interfering influence of other clock signals on the predetermined pixel frequency. See Gutttag, Col. 3, lines 3-5, Col. 55, lines 59-62.

Thus, Ishii in view of Gutttag fails to teach or suggest the present invention as recited in amended Claim 1. Applicant respectfully submits that amended Claim 1 is, therefore, in condition for allowance.

Amended Claim 7 recites, similar to amended Claim 1, an integrated video display system for providing a video signal having reduced beat patterns, comprising *inter alia* a video data circuit coupled to an output circuit through a latching circuit, the video data circuit being configured to provide a video data signal based on a pixel frequency, the pixel frequency being based on an external clock reference, the latching circuit being at a final stage of a video path between the video data circuit and the output circuit. Thus, for at least the same reasons as discussed above, amended Claim 7 is patentable over Ishii in view of Gutttag, and therefore in condition for allowance.

{S:\8211\000s081-us0\80003753.DOC [REDACTED] }

Application No.: 09/864,561

7

Docket No.: 08211/000S081-USO

Amended Claim 13 recites, similar to amended Claim 1, an integrated video display system for providing a video signal having reduced beat patterns, comprising *inter alia* a re-clocking circuit wherein interfering influence of other clock signals on the predetermined pixel frequency is removed if the re-clocking circuit is coupled at a final stage of a video path between the video data source and the output circuit. Thus, for at least the same reasons as discussed above, amended Claim 13 is patentable over Ishii in view of Guttag, and therefore in condition for allowance.

Claims 2-4, 11-12, and 14-16 are dependent from amended Claims 1, 7, and 13, respectively, and are patentable for at least the same reasons as stated for amended Claims 1, 7, 13, and therefore in condition for allowance.

The 35 U.S.C. §103(a) rejection of Claims 5, 6, 9, 10, and 17-20:

Paragraph 4 of the Office Action has rejected Claims 5, 6, 9, 10, and 17-20 under 35 U.S.C. §103(a) as being unpatentable over Ishii in view of Guttag and in further view of U.S. Patent No. 4,336,558 to Lew (hereinafter "Lew"). Applicant respectfully traverses this rejection.

The Applicants respectfully submit that the prior art references do not suggest or teach any of the claimed limitations. Claims 5, 6, 9, 10, and 17-20 depend from amended independent Claims 1, 7, and 13. As discussed above, Ishii in view of Guttag fails to teach or suggest the claimed invention as recited in amended Claims 1, 7, and 13. Furthermore, Lew discloses sampling scan lines with clock signals of different phases to produce a displacement between adjacent scan lines in the output image. See Lew, Abstract. Lew also fails to teach or suggest providing a local clock signal to re-clock the video data signal at a final stage of a video path between the video data signal circuitry and output circuitry, the local clock signal being based on the external clock reference, thereby removing interfering influence of other clock signals on the predetermined pixel frequency. See Lew, Fig. 1, 2.

Thus, Ishii in view of Guttag and in further view of Lew fails to teach or suggest the present invention as recited in amended Claims 1, 7, and 13. Applicant respectfully submits that

{S:\8211\000s081-us0\80003753.DOC [REDACTED] }

Application No.: 09/864,561

8

Docket No.: 08211/000S081-US0

Claims 5-6, 9-10, and 17-20 are dependent from amended Claims 1, 7, and 13, respectively, and are patentable for at least the same reasons as stated for amended Claims 1, 7, 13, and therefore in condition for allowance.

CONCLUSION

By the foregoing explanations, Applicant believes that this response has addressed fully all of the concerns expressed in the Office Action, and believes that it has placed each of the pending claims in condition for immediate allowance. Entry of the amendments and early favorable action in the form of a Notice of Allowance is urged. Should any further aspects of the application remain unresolved, the Examiner is invited to telephone Applicant's attorney at the number listed below.

Dated: March 3, 2004

Respectfully submitted,

By

John W. Branch

Registration No.: 41,633

DARBY & DARBY P.C.

P.O. Box 5257

New York, New York 10150-5257

(212) 527-7700

(212) 753-6237 (Fax)

Attorneys/Agents For Applicant

Attachments

{S:\8211\000s081-us0\80003753.DOC [REDACTED]}